REMARKS

Amendment to Claim 1

Applicant has corrected the grammar in claim 1 by switching the grammatically incorrect verb form of the verb 'connect' from "becomes to connect to" to the proper form "becomes connected to". No new matter is entered.

Claims 1 and 7 are rejected under 35 USC 103a as being unpatentable over Applicant's Admission of Prior Art (hereinafter AAPA) in view of Schnizlein (US Patent No 4,414,538, hereinafter SCHNIZLEIN)

Applicant asserts that claims 1 and 7 should not be found unpatentable over the AAPA in view of Schnizlein for at least the following reasons:

Concerning claim 1, applicant firstly asserts that neither the AAPA nor Schnizlein teach or suggest "a detect circuit electrically connected to the output end of the key cell for generating a control signal whenever the output end of the key cell becomes connected to the other of the second voltage and the first voltage", as claimed in claim 1 of the present invention.

The Examiner stated in the Office action mailed 10/18/2006 that "SCHNIZLEIN, analogous in art with AAPA, teaches/suggests a keyboard in Figure 1 comprising: a detect circuit (60,62) electrically connected to the output end of a key cell (16) for generating a control signal (on line 65) whenever the output end of the key cell becomes to connect to the other of a first state and a second state". However, the applicant respectfully disagrees. Looking at Figure 1 of Schnizlein it is clear that elements 60 and 62 are the analog comparator 60 and the debounce and validation logic 62, respectfully. The operation of these two units as taught by Schnizlein does not include any functionality similar to "generating a control signal whenever the output end of the key cell becomes connected to the other of the second voltage and the first voltage". Specifically, Schnizlein teaches starting at col 3, line 60 that "The sense conductor 24 feeds the sampled signal to a coding circuit 55 including an

analog comparator 60 functioning as a level slicer. When the signal on the sense line 24 falls below a fixed value which corresponds to a sensed, closed keyswitch 16a-y, the comparator 60 feeds a signal H to a debounce and validation logic unit 62 which also receives the clock signal C1. The debounce and validation logic 62 serves to distinguish between extraneous signals and valid key closures and provides a signal to a parallel to serial converter 64 via line 65."

Applicant notes that this functionality described for elements 60 and 62 by Schnizlein is not equivalent to the present invention as claimed in claim 1 because the comparator 60 of Schnizlein sends the signal H only when the signal on the sense line 24 is below a fixed value. Applicant notes that the sense line 24 in Figure 1 is generated according to which particular key 16a-y corresponds to the discharge transistor 50 having a gate being driven according to the output of the counters 32 and 18, shown respectively as the signals 45a-b and 31a-e in Fig.2. These counters are clocked by the clock signal C1. That is, at any particular time, the sense line 24 only corresponds to the current state of one of the keys 16a-y. The other keys can change state during this time and the sense line 24 will not indicate such change of state. Additionally, when the sense line 24 indicates a change of state (ie, a drop below the fixed value which corresponds to a sensed, closed keyswitch 16a-y), such a change of state does not correspond in time to when the output end of the key cell becomes connected to the other of the second voltage and the first voltage. Specifically, the output end of the key cell could have already become connected to the other of the second voltage and the first voltage much earlier in time but simply was not indicated on the sense line 24 because other keys were being sensed at that time. In effect, Schnizlein polls each of the key switches 16a-y one by one checking their respective states at the time of polling only. Therefore, applicant asserts that Schnizlein does not teach "a detect circuit electrically connected to the output end of the key cell for generating a control signal whenever the output end of the key cell becomes connected to the other of the second voltage and the first voltage", as claimed in claim 1 of the present invention because the sense line 24 is only effectively connected to one key 16a-y at a time and rotates through the keys one by one according to the clock signal C1 outputted

by clock unit 27. The circuitry taught by Schnizlein simply does not permit a control signal to be generated whenever the output end of the key cell becomes connected to the other of the second voltage and the first voltage. For at least this reason, applicant asserts claim 1 should not be found unpatentable over the AAPA in view of Schnizlein.

Concerning claim 7 of the present invention, applicant asserts a very similar argument also applies. Described briefly, claim 7 of the present invention includes "a detect circuit electrically connected to the output end of the key cell for detecting a transient voltage at the moment when the key cell is pressed or released and then generating a control signal". (emphasis added) However, as described above, the circuitry taught by Schnizlein simply does not permit a detecting a transient voltage at the moment when the key cell is pressed or released and then generating a control signal because the sense line 24 of Schnizlein is being cycled one by one through each of keys 16a-y according to the clock C1. That is, the moment the key cell is pressed or released will be missed for all keys not currently being selected for sensing by the sense line 24. Additionally, even when the sense line 24 does indicate a key is depressed, the signal change of the sense line 24 does not correspond to the moment when the key cell was pressed (or released). The key could have already been pressed much earlier in time but wasn't detected until the clock signal C1 and counters 32 and 18 cycled to sense that particular key. For at least this reason, applicant asserts claim 7 should also not be found unpatentable over the AAPA in view of Schnizlein.

Secondly, the Examiner combined the teachings of the AAPA and Schnizlein to render claims 1 and 7 of this application unpatantable. However, applicant would like to point out the contradiction in this combination. In the Schnizlein reference, the keyswitches are a scanned-type art (col. 1, lines 14, 45, and 66; col. 3, line 15; col. 4, lines 10, 12 and 38) and the circuit disclosed in the reference is simply used for a scanned-type keyswitshes (col. 1, lines 45-48, ...for scanning a plurality of keyswitches arranged in a matrix having a plurality of row conductors and a plurality of column conductors.) However, the key module 52 disclosed in the invention of the application, of which each of key cells (SW) has an output end being selectively connected to a first voltage (Vcc) and a second voltage (GND), is not a

scanned-type art, so that the circuit used in Schnizlein reference cannot be applied to combine with the AAPA in Fig.1 of the present invention. Therefore, applicant asserts there is in fact no motivation to combine the AAPA and Schnizlein to render claims 1 and 7 of this application unpatantable. Specifically, the circuit structure and operation of the reference of Schnizlein is not compatible with that of the AAPA so there is no motivation for one skilled in the art to combine the two. For at least this reason, applicant asserts claims 1 and 7 should not be found unpatentable over the AAPA in view of Schnizlein.

Thirdly, the applicant would like to emphasize that claimed features of the present invention, supported particularly in paragraph 0014, 0015, 0016, and 0017, as disclosed that when the key module is pressed or released, the output end of each of the key cell (switch) provides the input signals to the parallel-to-serial register, and the detect circuit detects a transient voltage formed in the capacitor and then outputs the control signal (CS) to the processor, are not taught by Schnizlein. In the other words, the detect circuit of the present invention detects voltage changes from the key cells (switches) to generate key-pressing/key-releasing signals (i.e. the control signal CS) to inform the processor and render the processor to request the parallel-to-serial register and read the data (input signals) stored therein. However, in the Schnizlein reference, "the detect circuit" believed by the examiner to be the analog comparator 60 and a debounce and validation unit 62 does not include any capacitors and the debounce and validation unit 62 serves to distinguish between extraneous signals and valid key closures and to provide a signal to a parallel-to-serial converter 64 via line 65 (col. 4, lines 2-5). In one embodiment of the present invention, the detect circuit comprising at least a capacitor is used to detect voltage changes from the corresponding key cell and does not filter any signals from the key module (Fig.2). Therefore, the analog comparator 60 and the debounce and validation unit 62, disclosed in Schnizlein reference, function in different way and perform a different task from the detect circuit in this claimed embodiment of the present invention. Accordingly, the applicant believes that the Examiner has no grounds to combine the AAPA and the Schnizlein reference to render claims 1 and 7 of this application unpatantable.

Fourthly, as described above, Schnizlein teaches that the debounce and validation unit 62 provides a signal to a parallel-to-serial converter 64 via line 65 (col. 4, lines 2-5). However, in the claimed invention, the detect circuit is not electrically connected to the parallel-to-serial register directly other than being electrically connected to the processor. The processor is electrically connected to the parallel-to-serial register for controlling it to conduct parallel-to-serial data transformation and read the data therein upon reception of the control signal from the detect circuit. Applicant therefore points out that Schnizlein discloses a circuit arrangement different from the claimed invention. In the Office Action mailed 10/18/2006, the Examiner argues that the processor is inherently suggested in the parallel-to-serial converter 64 (deemed as the same to the parallel-to-serial register by the Examiner) for processing decoder 66 output only in response to a signal from the detect circuit (i.e. analog comparator 60 and debounce and validation unit 62). However, the applicant respectfully disagrees with this argument and instead asserts that a person skilled in the art will realize that a parallel-to-serial converter 64 is simply a passive component which typically only responds to outer control signals to process decoding data. Parallel-to-serial converters do not normally include processors, and applicant also notes there are no explicitly written descriptions by Schnizlein suggesting the parallel-to-serial converter 64 comprises an inherent processor. Even as described by the Examiner that a processor is inherently suggested in the parallel-to-serial converter 64, the inherent processor appears to function for processing the parallel output of the ROM decoder 66 on cable 67 being converted a serial output by the converter 64 and sent to additional processing equipment (Ie. col. 4, lines 16-19), which is very different from that done by the processor in the claimed invention for controlling the parallel-to-serial register to conduct parallel-to-serial data transformation and read the data therein upon reception of the control signal from the detect circuit. Therefore, the applicant asserts that the parallel-to-serial register (converter) and the inherent processor believed to exist by the Examiner are different from those of the claimed invention in genuine functions. The applicant further asserts that because the whole circuit arrangement disclosed by Schnizlein is totally different from that of the present invention, a combination of Schnizlein

with that of the AAPA cannot be identical and function identical to the present invention.

Accordingly, the applicant believes that the Examiner has no grounds to combine the AAPA and the Schnizlein reference to render claims 1 and 7 of this application unpatantable. Even if combined, as described above, applicant asserts that it is impossible for the person skilled in the art to achieve the same functions and components as claimed in the present invention claims 1 and 7 without further inventive process. The reason is that a key feature of the Schnizlein reference (ie, cycling/polling through each of the keys one by one) is not compatible with generating a control signal at the moment the key is pressed or released, as is claimed in the present invention. For at least the above described reasons, applicant asserts claims 1 and 7 of the present invention should be found patentable over the AAPA combined with Schnizlein reference. Reconsideration of claims 1 and 7 is respectfully requested. Claims 2-6 and 8-15 are dependent upon claims 1 and 7 and should therefore be found allowable for at least the same reasons.

Claims 2,3 and 8-10 are rejected under 35 USC 103a as being unpatentable over Applicant's Admission of Prior Art in view of Schnizlein as applied to claims 1 and 7 above, and further in view of Hackmeister (US Patent No. 4,027,306, hereinafter HACKMEISTER)

As mentioned above, claims 2,3 and 8-10 are dependent upon claims 1 and 7, respectively, which are believed to be allowable for the above stated reasons. Therefore, claims 2,3 and 8-10 should also be found allowable for the same reasons as their base claims.

Additionally, applicant would also like to point out that the Hackmeister reference discloses an ohmic contact 13', being not an ordinary key cell (switch) like that either in AAPA or in the Schnizlein reference. The ohmic contact 13' induces small voltage by electromagnetic fields present in the environment when a person touches (col. 4, lines 9-11). For this reason, applicant asserts there is no ground to combine the teachings of Hackmeister with AAPA, and there is also no suggestion/motivation to integrate the teachings of the Hackmeister reference with a combination of AAPA and Schnizlein reference, if such a

combination may be established, to achieve the claimed invention. For at least reasons, claims 2, 3, 8 and 10 of the present invention should not be found unpatentable over the AAPA in view of Schnizlein, and further in view of Hackmeister. Reconsideration of claims 2, 3, 8, and 10 is respectfully requested.

Claims 4-6 and 11-15 are rejected under 35 USC 103a as being unpatentable over Applicant's Admission of Prior Art, Schnizlein and Hackmeister as applied to claims 1-3 and 7-10 above, and further in view of Johnson (US Patent No. 6,265,993 B1, hereinafter JOHNSON)

As mentioned above, claims 4-6 and 11-15 are dependent upon claims 1 and 7, respectively, which are believed to be allowable for the above stated reasons. Therefore, claims 4-6 and 11-15 should also be found allowable for the same reasons as their base claims.

New claims 16 and 17

Applicant has added new claims 16 and 17 based on claims 1 and 7, respectively. The difference between the new claims and their corresponding original claims is that further limitations of the processor are added. Specifically the processor is also for reading the input data therein according to reception of the control signal. No new matter is entered.

Concerning the patentability of new claims 16 and 17 with respect to the above cited reference of Schnizlein, applicant again notes that such an inherently suggested processor as assumed to exist by the Examiner in the parallel-to-serial converter 64 appears to only function for processing the parallel output of the ROM decoder 66 on cable 67 being converted a serial output by the converter 64 and sent to additional processing equipment (Ie. col. 4, lines 16-19), which is very different from that done by the processor in the claimed invention for controlling the parallel-to-serial register to conduct parallel-to-serial data transformation and read the data therein upon reception of the control signal from the detect circuit. That is to say, the inherent processor controls the converter 64 to send

parallel-to-serial transformed data to additional processing equipment while the processor of the present invention is simply for reading parallel-to-serial transformed data sent from the parallel-to-serial register. Therefore, the applicant asserts that the parallel-to-serial register (converter) and the inherent processor believed to exist by the Examiner are different from those claimed in claims 16 and 17. Consideration of claims 16 and 17 is respectfully requested.

Sincerely yours,

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